11

Design Conversion

11.1 Introduction

In CADIC there are a lot of interfaces to convert its internal netlist format into the exchange formats of commercial design systems. With the help of these interfaces the designer can use the advantages of the graphical editor, especially its parametric design methods, in a comfortable graphical frontend.

The conversion tool in CADIC can generate different exchange formats out of the graphical specification of a circuit. The tool works on the DAG structure, from which it first builds a representation in form of a hierarchical netlist. In addition to the Cgraph structure each treenode in the DAG holds a pointer to a netlist data structure for the corresponding hierarchy level. Because some of the generated formats do not support a hierarchical description, we have to expand the hierarchy into a flat netlist. This operation can be done by an additional tool which can be called before the exchange format is written to the output file (c.f. figure 11.1).

The hierarchical netlist data structure in CADIC contains all informations needed to create all usual exchange formats. The structure of these formats can be classified into the following two groups:

- *cell list*: In the case of a flat netlist description this list only contains the names of the basic cells in the design. Within a hierarchical format this list contains the macros and basic cells for each hierarchy level.

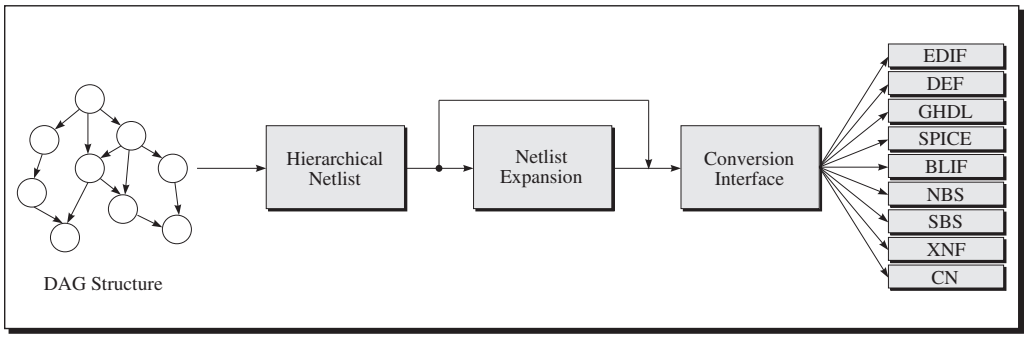


Figure 11.1: Components for generating exchange formats

- *logical connection*: The description of the connections between the cells bases on one of the following schemes:
  - *net oriented netlist*: The structure of the logical interconnections is described by a list of signal nets. For each net of this list it is denoted which pins of cells it combines.
  - *cell oriented netlist*: In this case the structure is given by a list of macros and basic cells. For each element of this list, the identifiers of the corresponding signal nets at its pins are denoted.

Beside the functional description of a design some exchange formats also support the specification of structural informations. For example this can be used to describe clusters of cells, which have to be placed in the same area. In our case this could be used to pack one hierarchy level in one cluster.

11.2 Supported Formats

As you can see from figure 11.1 CADIC currently supports the following exchange formats:

- *EDIF 2 0 0*: The exchange format EDIF (Electronic Design Interchange Format,[Com87]), developped from the Electronic Industries Association, meanwhile has established as standard format which is used in a lot of commercial desgin systems (e.g. Cadence Design

System,[CAD92]).

- *DEF*: The design system TANGATE ([SYS90]) uses the format DEF (Design Exchange Format) which has been defined by TANGENT SYSTEMS for the exchange of design data between the different tools in TANGATE.

- *GHDL*: The system HILO from GenRad ([Gen90]) contains the tools HISIM, HIFAULT and HITIME for different simulation models of integrated circuits. The input of a design to this system is done in form of a GHDL (GenRad Hardware Description Language) file, which is hierarchically organized.

- *SPICE*: The SPICE format has been developped for the circuit simulation program SPICE from the University of California, Berkeley.

- *BLIF*: The format BLIF is the input format for the logic synthesis tools in the OCTTOOLS package which has been developped by the University of California, Berkeley.

- *NBS*: The format NBS and the modified format NBS(f) are used within the layout system HULDA ([?]) from the Humboldt University of Berlin.

- *SBS*: With SBS (Strukturbeschreibungssprache) the graphical editor can be used as frontend for the design system VENUS from SIEMENS. It also can be used to address the logic simulator SMILE. In order to use this format the design has to be developped with the basic cell libraries ACMOS3 or ACMOS4. The ACMOS4 library is delivered with the basic CADIC distribution.

- *XNF*: The format XNF (Xilinx Netlist Format) is the netlist format of the XACT system which is a popular FPGA (Field Programmable Gate Arrays) development system from the Xilinx Company. With this conversion interface, a CADIC design can be transformed to the XACT system in order to realize the design with the FPGA technology.

- *CN*: The format CN is an alternative to SBS in order to give a CADIC design to the VENUS system. This format is used by the graphical editor SIGRED and from the layout subsystem in VENUS.

For a documentation of the structure of these different formats you should look at the corresponding manuals. For the following the syntax of the formats is not important.

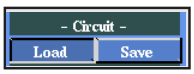
11.3 Design Conversion

In order to activate the design conversion, you should select the entry `Netlist Formats` from the submenu `-Converter-` within the main menu of CADIC . Then a new submenu, named `Converter` is displayed, and you are in the mode of the function selection.

The conversion routines create files for the different exchange formats. Theses files are placed in directories given by some environment variables. For example the files created by the EDIF converter are located in a directory which is given by the environment variable `EDIFDIR`. The formats with the corresponding enviroment variables are listed below. Note, that you must have write permission for these directories. If you do not want to distinguish between the different formats you can set all the variables to the same directory as it is done in the example shell scripts in the CADIC distribution.

⇝ 3

Load Circuit

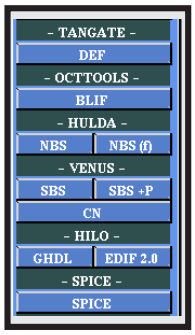


If you want to convert the internal representation of a CADIC circuit into other formats, you must first load its DAG data structure. As shown in the previous chapters this can be done with the entry `Load` from the submenu `-Circuit-`.

⇝ 5.2.1

In this section we will load the 16 bit conditional sum adder and transform it to various exchange formats. To load this adder you should select the entry `CSA[n]` from the circuit list window and type in `16` as the parameter value in the following input window.

Convert Design



In the `Converter` menu the netlist formats are placed under the corresponding name of the design system. For example, the format `DEF` is placed under the system name `-TANGATE-`. The format `EDIF 2 0 0` is placed under the system name `-HILO-`, because EDIF can also be used as input for the simulation package HILO.

After loading the hierarchy of a circuit you can now choose the desired exchange format. Then simply press the push button of the required netlist format. After calling the corresponding conversion routine the system will display a list of informations in the message window. The type of messages depends on the selected format.

For example we will now convert the loaded 16 bit conditional sum adder into the DEF format for the TANGATE design system. To do this select the entry `DEF` from the `-TANGATE-` submenu. In the message window you will see the following informations:

```
start of generating netlist for CADENCE
READY: netlist for CADENCE has been generated
```

The file of the generated format is put in the directory given by the environment variable `CADENCEDIR`. The file has the name `CSA0160.def`, i.e. the suffix of the created file corresponds to the exchange format. In some cases the square brackets and the commas in the parameter list of the circuit are replaced by other characters. In this case of the DEF format they are replaced by `0`. This replacement is done for the formats DEF, BLIF, NBS and SPICE. For GHDL the square brackets and commas are replaced by _.

The suffixes and their corresponding format names are grouped in the following way:

- DEF: `<name>.def` in `CADENCEDIR`
- BLIF: `<name>.netblif` in `EDIFDIR`
- NBS: `<name>.nbs` in `NBSDIR`

- NBS(f): `<name>.nbf` in `NBSDIR`
- GHDL: `<name>.cct` in `HILODIR`
- EDIF 2.0: `<name>.edif` in `EDIFDIR`
- SPICE: `<name>.cir` in `EDIFDIR`
- XNF: `<name>.xnf` in `EDIFDIR`

Here we will continue the example of the 16 bit conditional sum adder. We will now convert the DAG structure into an EDIF file. To do this select the entry `EDIF 2.0` from the submenu `-HILO-`. After activating the push button the system will display the following informations:

```
gen_edif:  Start Generation for CSA[16]
( header basiccells macrocells )
Done.
```

For small circuits as this example the generation of the exchange formats is done immediately. If you load a larger design (e.g. 256 bit conditional sum adder) this process will take more time and you can see the different sections of the generation process being displayed in the message window.

For the EDIF format the created file is in the directory `EDIFDIR`. It has the name `CSA[16].edif`, i.e. in the case of EDIF the square brackets and the commas in the parameter list are not replaced by other characters.

Changing the View

With the help of the functions from the submenu `-Views-` you can change the graphical representation of the schematic. The functions in the menu of the netlist conversion tool are identically to those in the hierarchy menu. For an explanation you can look at section 5.9.

To terminate the conversion menu you have to terminate any currently active function first. In most cases this can be done by pressing the right mouse button at most twice within the workarea (see also the description of the appropriate function). After that you are in menu selection mode

and you can close the conversion menu by pressing the right mouse button within the menuline. Now you return to the main menu of the CADIC system. From there you can select another tool or you can terminate the whole system call by selecting the entry `Exit` in the main menu.