Two-layer wiring with pin preassignments is easier if the power supply nets are already generated

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Abstract

We examine the constrained via minimization problem with pin preassignments (CVMPP) which arises in connection with hierarchical physical synthesis. Let A be a circuit composed of subcircuits B, C, D, ... Assume that the placement and routing phase together with the 2-layer wiring of the subcircuits, and the placement and routing phase without the 2-layer wiring of A are completed. CVMPP is the problem of finding a 2-layer wiring δ_A of A which is induced by the 2-layer wirings of the subcircuits and which contains a minimal amount of vias on this condition. First, we show that CVMPP is NP-hard. In the case that the wiring of the power supply nets has already been generated we present a polynomial time algorithm solving CVMPP.

1 Introduction

Today's integrated circuits have up to several hundred thousand transistors. Processing such designs in a naive manner requires very large internal representations with some millions of data so that even linear space (time) optimization algorithms can be too expensive. However, large designs have a regular structure. In such arrangements, there are lots of identical subcircuits so that they can be described by small hierarchical representations. During synthesis, it is desirable to handle all instances of a subcircuit identically in order to guarantee identical electrical behavior of all instances, to allow further hierarchical processing and to decrease the running time of the synthesis.

Hierarchical physical synthesis is not highly developed yet. Results on hierarchical compaction can be found in [4, 10]. Results concerning the hierarchical physical design of systolic arrays are presented in [5, 6]. Some new results taking advantage of buses during hierarchical wiring appeared in [8].

A leading feature of VLSI design systems is the placement and routing aspect. Typically, routing consists of two steps: *wire layout* and *wiring* (*layer assignment*). The first step determines the placement of the routing segments. A 'planar' wire layout is obtained. In the wiring step, this layout is converted into an actual three-dimensional configuration of wires. Formally, wiring is formulated as follows: Given a wire layout L and k physical layers, assign each routing segment of L a unique physical layer in a way that the segments are electrically connected in the proper way. Adjacent edges of the same wire lying on different layers are connected with vertical connections, called *vias*. Segments of different wires crossing each other have to be assigned to different layers. A problem arising in this context is the *constrained via minimization problem* (kCVM), i.e., computing a k-layer wiring with a minimal number of vias. Minimizing the number of vias is a step towards optimizing the performance of the circuit and decreasing its manufacturing costs. The k-layer wiring problem, especially the kCVM for non-hierarchical circuits has been comprehensively investigated in the literature. A survey on these results is given in [7].

In this paper, we concentrate on 2CVM (which we denote by CVM in the following) and address the following problem. Let A be a circuit composed of basic cells whose input and output pins lie in a certain but fixed layer (ALU1 or ALU2). Assume that the placement and routing phase is already completed. Find a 2-layer wiring of the wire segments of A such that each wire segment is embedded either into ALU1 or ALU2, the pins of the basic cells lie in the preassigned layers, and the number of vias is minimal on these two conditions. A solution of this problem which we denote by CVMPP (**c**onstrained **v**ia **m**inimization with **p**in **p**reassignment) induces a hierarchical bottom-up 2-layer wiring algorithm which preserves the original layout hierarchy of the circuit.

For this, we need the following definitions.

Definition 1 *A circuit or a macro cell is said to be of level* 1 *if it contains no macro cell but only basic cells, and is said to be of level $i+1$ if it contains at least one macro cell of level i and no macro cell of level greater than i.*

Definition 2 *Let A be a circuit of level i composed of basic cells and macro cells B, C, D, ... which are interconnected by some wire layout. Let δ_B, δ_C, δ_D, ... be 2-layer wirings of B, C, D, ..., respectively. A wiring δ_A of A is said to be induced by δ_B, δ_C, δ_D, ... if δ_A is given by applying δ_X on all occurrences of X $(X \in \{B, C, D, \ldots\})$ and then realizing the 2-layer wiring of the interconnecting wire layout.*

Hence, the CVMPP problem can be expressed as follows:

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Given 2-layer wirings δ_B, δ_C, δ_D, ... of the (basic cells and) macro cells B, C, D, ..., respectively.

Find a 2-layer wiring δ_A of circuit A induced by δ_B, δ_C, δ_D, ... which has less (or equal) vias than any other 2-layer wiring δ'_A of A induced by δ_B, δ_C, δ_D, ...

A first suggestion for solving CVMPP in polynomial time has been made by Pinter [9]. But his procedure is only applicable if the preassignments are restricted to exterior pins (located at the outer border of the routing area), a condition normally not fulfilled by hierarchical circuit representations. Grötschel et al. [2] generalized Pinter's procedure to deal with arbitrary pin preassignments. They reduce CVMPP to the **max-cut** problem for **a**lmost **p**lanar **g**raphs (MCAPG), i.e., graphs which can be transformed into a planar graph by removal of only one node. Since MCAPG has been shown to be NP-hard [1], CVMPP is not solved exactly in [2] but attacked by approximation techniques from combinatorial optimization.

Grötschel's procedure implies the following question: Is it adequate to solve CVMPP by heuristics or does there exist a fast exact algorithm? In Section 3 we prove that CVMPP is NP-hard, thus shattering hopes for a fast exact solution. The proof is done by showing the opposite direction to Grötschel's reduction, i.e., reducing MCAPG to CVMPP.

Clearly, the fact that CVMPP is NP-hard in general does not exclude exact polynomial time algorithms for important special cases. Section 4 characterizes such an important subclass of wiring problems. We restrict to designs with power supply nets routed in layers ALU1 and ALU2, and assume that the layer assignment for power and ground has been fixed before wiring the signal nets. It is shown that under these assumptions CVMPP can be solved as efficiently as CVM, which is known to be solvable in time $O(n^{3/2}\log n)$ (if the maximum junction degree, i.e., the maximum number of wire segments which meet at a single point, is limited to three) where n is the sum of the wire lengths of the layout (see [3]).

2 A heuristic for CVMPP

In this section we review the heuristic for CVMPP presented in [2] which is based on Pinter's model [9].

2.1 Pinter's solution to CVM

As already mentioned, we assume that all cells have been placed on a chip and all nets have been routed but that the assignment of wire segments to layers has not been performed yet. Let W denote the wire layout. Obviously, each wire is partitioned into free and critical segments such that vias are allowed on free but forbidden on critical segments. A cluster is defined to be a maximal set of mutually crossing and overlapping critical wire segments. Obviously, in each cluster, once a wire segment is assigned to a certain layer, wiring of the rest of the cluster is forced. In addition, a 2-layer wiring exists if and only if every cluster is 2-layer wireable because the clusters are connected to each other by free segments, where vias are allowed.

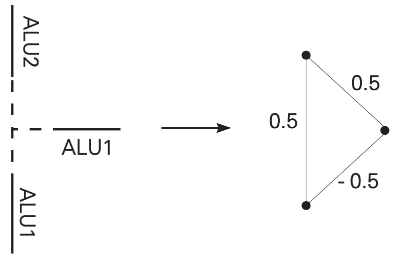

Figure 1: Modelling of a three-way junction. Dashed (solid) lines denote free (critical) segments.

Now, to find a solution to CVM, Pinter proceeds [9] as follows. The clusters form a planar graph called cluster graph. Each vertex of the graph corresponds to a cluster and two vertices are connected by an edge if and only if their corresponding clusters are connected to each other by at least one free wire segment. Now assume that a 2-layer wiring δ of W is given. Then a weight $\omega(e)$ is associated to every edge e of the cluster graph in the following way. Let $v(e)$ be the number of free wire segments connecting the two clusters incident to e and let $\rho(e)$ be the number of vias introduced (on these free segments) by the wiring δ. Then, $\omega(e) = \rho(e) - (v(e) - \rho(e))$ indicates the via reduction that can be achieved by flipping over either one of the two clusters, i.e., by reassigning all the wire segments of either one of the two clusters to the opposite layer.

This reduction only works for two-point nets. If a net connects more than two terminals, there are junctions in the wire layout. Most commonly three way junctions are used. As vias are allowed to be inserted on a junction, Pinter [9] handles three-way junctions by replacing each junction by the subgraph shown at the right of figure 1. The three vertices represent the 3 clusters corresponding to the critical wire segments adjacent to the junction. The weights contributed by the junction itself are either -0.5 or 0.5 depending on whether the two corresponding critical wire segments are embedded in the same layer by wiring δ or in different layers by δ.

Obviously, any 2-layer wiring δ' can be obtained from a known wiring δ by flipping over an appropriate set $X(\delta, \delta')$ of clusters. If e is an edge of the cluster graph incident to clusters both in $X(\delta, \delta')$ or both not in $X(\delta, \delta')$, the number of vias between the two clusters remains unchanged. Otherwise, the number of vias is reduced by $\omega(e)$. (Note that the weights $\omega(e)$ can be positive or negative!) So, let X be any subset of the clusters and let $CUT(X)$ be the set of those edges of the cluster graph which connect vertices in X and vertices not in X. Then in order to minimize the number of vias, one has to find a subset X of the clusters such that $\sum_{e \in CUT(X)} \omega(e)$ is maximized.

Figure 2 shows an example wire layout W with two embedded modules. The critical (free) interconnection wire segments are drawn as solid (dashed) lines. The initial two-layer wiring δ of W is given by the numbers which specify for each cluster the layer of its horizontal wire segment. Obviously, the number of vias (marked by arrows) induced by δ is three. The cluster graph obtained by Pinter's procedure is given in Figure 3. The relative position of the cluster nodes is the same as that of the corresponding clusters in Figure 2. A maximum cut of weight 1 is obtained by choosing $X = \{5, 6, 7\}$ (the corresponding edges are drawn bold in Figure 3). The layer assignment δ' obtained from δ by flipping the nodes of X thus needs only two vias, which is optimal.

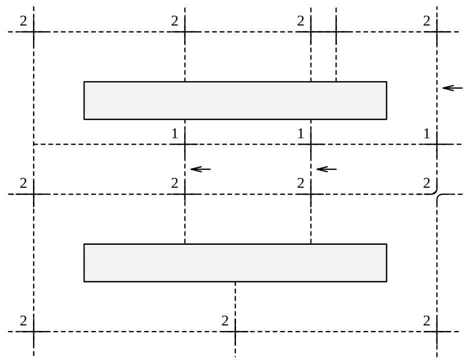

Figure 2: Layout without pin preassignments

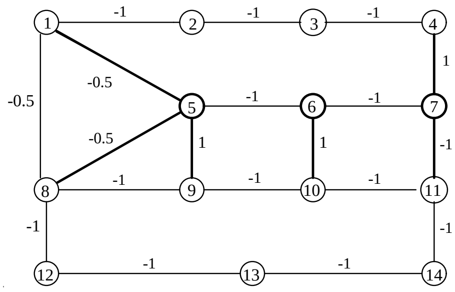

Figure 3: Cluster graph and maximum cut

If the maximum junction degree of the wire layout W is limited to three, it is easy to see that the cluster graph is planar (see [9]). Hence, CVM for this case is reduced to the **m**aximum **c**ut problem for **p**lanar **g**raphs (MCPG) with arbitrary weights, which is solvable in time $O(n^{3/2} \log n)$ where n is the sum of the wire lengths of the layout W.

2.2 Grötschel's heuristic for CVMPP

Pinter already sketched a procedure for incorporating pin preassignments into his approach. He suggested to introduce edges of large absolute weight between pins. Hence, his algorithm was forced to preserve relations between preassigned layers. Planarity of his extended cluster graph was only guaranteed if all preassigned pins were located at the outer border of the routing area. Thus, Pinter reduced CVMPP to the **m**aximum **c**ut problem for nonplanar graphs (MC) which is NP-hard.

Grötschel et al. [2] reduce CVMPP to MCAPG by the following straightforward procedure. Let W be an arbitrary wire layout with pin preassignments. Assume w.l.o.g. that we are not allowed to place vias at pins. Thus, for each preassigned pin a critical wire segment starting at that pin is introduced. A new rule is added for clustering which demands that all critical wire segments corresponding to pins are assigned to the same cluster. As a result, we obtain a singular cluster c_0 consisting of all critical pin wires and the critical lines which are crossed or overlapped by them. Let δ be an arbitrary wiring of W meeting the pin preassignments. Then, the definition of the cluster graph and its edge-weights with respect to δ is analogous to that described in the previous subsection.

Solving CVMPP is then equivalent to solving MC for the resulting cluster graph. To see this, assume for a moment that the wiring of c_0 can be flipped. Then, by the same argumentation as in Pinter's approach, we conclude that a maximal cut X corresponds to an optimal layer assignment δ' obtained from δ by flipping over the clusters from X. If δ' flips all wires of c_0 to the wrong layer, i.e., $c_0 \in X$, we simply take its dual version which has the same number of vias and meets the preassignments of c_0.

Figure 4 shows our example wire layout extended by pin preassignments, which are given by numbers at the module borders. The critical line segments belonging to cluster c_0 are drawn in bold. Note, that clusters 5 and 6 are 'absorbed' by cluster c_0, since there is no free wire segment connecting to the corresponding pins. In this example, the initial wiring δ is given by the optimum solution of the previous example shown in Figures 2 and 3 illustrating Pinter's algorithm for CVM. This 2-layer wiring δ has been extended by the wiring of c_0 which is selected in accordance with pin preassignments. Since the optimum solution for CVM does not match well to the pin preassignments, δ induces a lot of vias, namely seven, which are marked by arrows in Figure 4. The corresponding cluster graph is given in Figure 5. Clearly, this graph is *not planar* (apply Kuratowski's characterization of planar graphs). A maximum cut of weight 3 is obtained by choosing $X = \{1, 2, 3, 4, 7\}$ (the corresponding edges are drawn bold in Figure 5). The optimum layer assignment δ' obtained from δ by flipping the nodes of X thus needs only four vias.

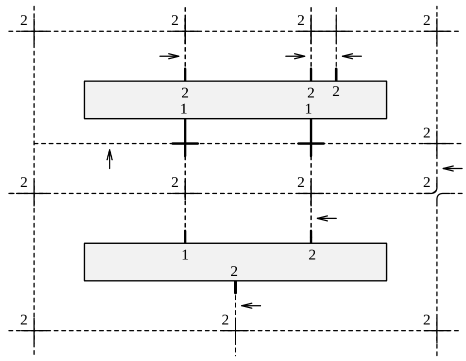

Figure 4: Layout with pin preassignments

As illustrated by the above example, the cluster graph

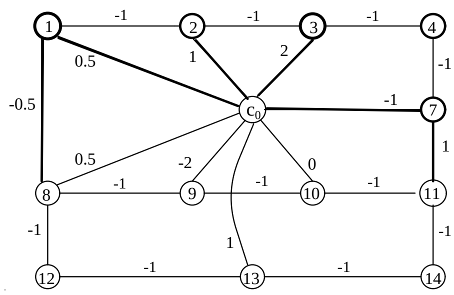

Figure 5: Non-planar cluster graph with maximum cut

for CVMPP need not be planar but clearly becomes planar if we remove c_0. Thus, the reduction results in a **m**ax **c**ut problem for **a**lmost **p**lanar **g**raphs (MCAPG). Unfortunately, MCAPG has been shown to be NP-hard by Barahona [1]. As a consequence, Grötschel's reduction only makes sense if CVMPP is not easier to solve than MCAPG. In the next section it will be proven that both problems are equivalent. Thus, Grötschel's heuristic is really adequate.

3 CVMPP is NP-hard

We present a reduction of MCAPG to CVMPP. Let $G = (V, E, \omega)$ be a weighted almost planar graph with $\omega : E \rightarrow \mathbf{Z}$. Let $v_0 \in V$ be a vertex such that the weighted graph $G_{pl} = (V_{pl}, E_{pl}, \omega_{pl})$ defined by $V_{pl} = V \setminus \{v_0\}$, $E_{pl} = E \cap (V_{pl} \times V_{pl})$, and $\omega_{pl} = \omega\mid_{E_{pl}}$ is planar. We will show that there exists a circuit C ($=C(G)$) where the pins of the macro cells are preassigned and a 2-layer wiring δ of C requiring ω_δ vias such that there is a cut CUT of G with weight ω_{CUT} if and only if a two-layer wiring δ' requiring $\omega_{\delta'} = \omega_\delta - \omega_{CUT}$ vias can be obtained from δ by flipping a certain subset $X(CUT)$ of the clusters of C.

Circuit C consists of two parts which are corresponding to G_{pl} and the edges adjacent to v_0, respectively. We start with the part corresponding to G_{pl}. We construct a wire layout W_{pl}, which does not contain any macro cell, by exploring G_{pl} in a breadth-first-search manner. Let χ be a planar embedding of G_{pl}, $v \in V_{pl}$ be a vertex, and $v_1, \ldots, v_{h_v} \in V_{pl}$ be the vertices adjacent to v in the clockwise direction with respect to χ (by starting with any vertex v_1 adjacent to v). Furthermore, let ω_i denote the weight $\omega(\{v, v_i\})$ for all $i \in \{1, \ldots, h_v\}$. We associate to v a wire layout W_v ($= W_v^{(h_v)}$), which only consists of critical wire segments, in the following way (see Figure 6). Assume inductively that for a given i the edges $\{v, v_j\}$ $\forall j \leq i$ are already explored and that the subcircuit $W_v^{(i)}$ of W_v and the 2-layer wiring δ restricted to $W_v^{(i)}$ is already constructed. Furthermore, assume that $W_v^{(i)}$ only consists of critical wire segments, and that it has exactly one horizontal wire segment at its right side. In the following, we denote the layer in which this horizontal wire segment is embedded by $\delta(W_v^{(i)})$.

During the exploration of edge $\{v, v_{i+1}\}$ we extend subcircuit $W_v^{(i)}$ to $W_v^{(i+1)}$. We distinguish between the following two cases.

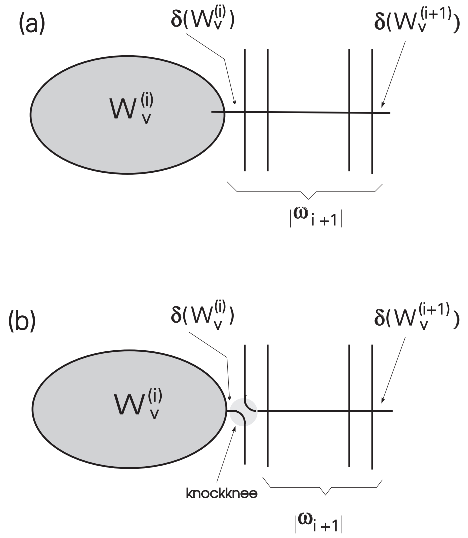

Figure 6: Illustration of the transformation of G_{pl}.

Case 1 The circuit $W_{v_{i+1}}$ corresponding to vertex v_{i+1} has not been constructed yet. Then $W_v^{(i+1)}$ is given by the wire layout shown in Figure 6 (a). The new wire segments are defined to be critical, too. Thus, $\delta(W_v^{(i+1)}) = \delta(W_v^{(i)})$.

Case 2 $W_{v_{i+1}}$ has already been constructed. Let v be the jth neighbor of v_{i+1}. If $\delta(W_{v_{i+1}}^{(j)}) = \delta(W_v^{(i)})$ and $\omega_{i+1} < 0$ (case 2.1.1) or $\delta(W_{v_{i+1}}^{(j)}) \neq \delta(W_v^{(i)})$ and $\omega_{i+1} > 0$ (case 2.1.2) then $W_v^{(i+1)}$ is given by the wire layout shown in Figure 6 (a) once again. The new wire segments are defined to be critical. Thus, $\delta(W_v^{(i+1)}) = \delta(W_v^{(i)})$. The new vertical wire segments are connected to the corresponding vertical wire segments of $W_{v_{i+1}}$ (more precisely, $W_{v_{i+1}}^{(j)} - W_{v_{i+1}}^{(j-1)}$) by free wire segments. Note that these connections can be done without crossing other connections because of the planarity of G_{pl}. Obviously, the 2-layer wiring δ introduces no via on the wire segments connecting $W_{v_{i+1}}^{(j)}$ and $W_v^{(i+1)}$ in case (2.1.1). Flipping either W_v or $W_{v_{i+1}}$ results in additional $-\omega_{i+1}$ vias on these free wire segments. In case (2.1.2), δ introduces ω_{i+1} vias onto these wire segments. Flipping either W_v or $W_{v_{i+1}}$ results in a saving of ω_{i+1} vias (on these connections). If $\delta(W_{v_{i+1}}^{(j)}) \neq \delta(W_v^{(i)})$ and $\omega_{i+1} < 0$ (case 2.2.1) or $\delta(W_{v_{i+1}}^{(j)}) = \delta(W_v^{(i)})$ and $\omega_{i+1} > 0$ (case 2.2.2) then $W_v^{(i+1)}$ is given by the wire layout shown in Figure 6 (b). The new wire segments are defined to be critical. Thus, $\delta(W_v^{(i+1)}) \neq \delta(W_v^{(i)})$ because of the knock-knee introduced. The new vertical wire segments are connected to the corresponding vertical wire segments of $W_{v_{i+1}}$ by free wire segments. These connections can be done without crossing other connections because of the planarity of G_{pl}.

The induction base is given by a subcircuit $W_v^{(0)}$ consisting of one horizontal critical wire segment with $\delta(W_v^{(0)})$ =ALU1. By the above discussion, it is obvious that there is a cut CUT of G_{pl} with weight ω_{CUT} if

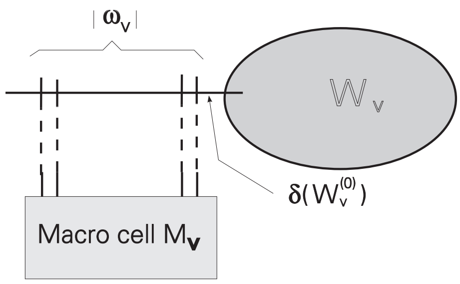

Figure 7: Transformation of edge $\{v, v_0\}$. Dashed lines denote free wire segments.

and only if there is a 2-layer wiring δ' ($= \delta'(CUT)$) with $\omega_{\delta'} = \omega_\delta - \omega_{CUT}$.

To finish our construction, we only have to consider vertex v_0. Let $e = \{v, v_0\} \in E$ be any edge incident to v_0 and ω_v be the corresponding weight. Remember that $\delta(W_v^{(0)})$ =ALU1, i.e., the horizontal wire segment at the left of W_v is embedded into ALU1 by the 2-layer wiring δ. Once again, we distinguish between the two cases.

Case 1: $\omega_v > 0$, i.e., the weight of a cut CUT increases by ω_v if $e \in CUT$. Thus, the wire layout we have to construct must have the property that flipping W_v locally results in a saving of ω_v vias. The construction shown in Figure 7 guarantees this requirement. The macro cell M_v has ω_v pins at its top border. The pins are preassigned to ALU1. Thus, the 2-layer wiring δ introduces a via for each pin. By flipping W_v, these ω_v vias can be removed.

Case 2: $\omega_v < 0$, i.e., the weight of a cut CUT decreases by $-\omega_v$ if $e \in CUT$. Thus, the wire layout we have to construct must have the property that flipping W_v implies that additional $-\omega_v$ vias have to be introduced. The construction shown in Figure 7 guarantees this demand if the pins of the macro cell M_v are preassigned to ALU2.

This completes the construction of circuit C and the 2-layer wiring δ. By the above discussion the following lemma holds.

Lemma 1 *There is a cut CUT of G with weight ω_{CUT} if and only if a two-layer wiring δ' of C requiring $\omega_{\delta'} = \omega_\delta - \omega_{CUT}$ vias can be obtained from δ by flipping a certain subset $X(CUT)$ of the clusters of C.*

Theorem 1 *CVMPP is NP-hard.*

Proof: It follows immediately from the results of Barahona ([1], Section 4.3) that MCAPG is NP-hard even if only graphs with edge weights bounded by a constant are considered. Thus, by the above construction we can reduce MCAPG to CVMPP in polynomial time. ■

4 ... if the power supply nets are already generated

In the last section it has been shown that the unrestricted CVMPP problem is NP-hard. Thus, we can not hope to find an optimum solution in polynomial time. Fortunately, in practice we often do not have to solve the general problem, but are confronted with technical constraints. As will be shown, such constraints may drastically simplify the problem, allowing for a polynomial time exact solution of the restricted optimization problem.

Let us consider the situation where not only the signal nets but also all power supply nets have to be laid out in ALU1 and ALU2. The routing of these nets is extremely critical because of voltage drop and current density constraints, and thus, vias on these wire segments are much more 'expensive' than signal wire vias. As a consequence, power and ground wiring is best done in advance, without consideration of signal nets. The subsequent signal wiring phase then has to meet the fixed wiring of power supply lines. This strategy considerably simplifies the solution of CVMPP, especially, we will show that:

Theorem 2 *Assume that the wiring of power supply nets has already been performed and must be met by the wiring of the signal nets. Then, CVMPP can be reduced to MCPG in linear time, and thus solved in time $O(n^{\frac{3}{2}} \log n)$.*

Proof: Let W be an arbitrary wire layout with pin preassignments and given power and ground wiring. Since the layer assignment of power supply nets is not allowed to change, we have to treat these nets in the same manner as preassigned pins. Thus, power and ground lines are considered as critical wire segments and all these wire segments are assigned to cluster c_0. Clearly, by the same argumentation as for the pin preassignment problem, solving MC for the resulting cluster graph G_W is equivalent to solving CVMPP for fixed power and ground wiring.

The NP-hardness of CVMPP was due to the non-planarity of G_W. But under the constraint of fixed power supply net wiring, it can be shown that G_W is always planar and thus CVMPP can be solved in time $O(n^{\frac{3}{2}} \log n)$ [3]. To see this, let us start by a simple observation based on the fact that every macro cell must be supplied with power and ground from the circuit borders: Let l be an arbitrary critical wire segment belonging to cluster c_0. There exists a path P (in the graph-theoretical sense) from l to a primary output of W which only passes through wire segments from c_0 and inner faces of modules.

Now, consider a rectangular layout W' which results from blowing up W such that all wires obtain non zero width. By definition, all the clusters except c_0 occupy a continuous area in W'. Let us assume that the inner faces of modules and the plane surrounding W''s rectangle are added to the area covered by c_0. Then, because of our observation above, c_0's area is also continuous.

The planar embedding of the cluster graph G_W is obtained by the following simple procedure: A cluster node is placed inside the area occupied by the corresponding cluster. The edges between the cluster nodes are drawn in two steps. First, we connect the corresponding cluster areas by following a free wire segment which induced the edge. These connections are obviously planar. Then, we draw the connections from the border of a cluster area to its cluster node. Since all cluster areas are continuous, this can also be done in a planar manner. ■

Figures 8, 9 and 10 illustrate the procedure of the above proof for our example circuit which has been extended by power and ground connections (extra bold lines) for both modules. The power supply lines are all treated as critical and belong to cluster c_0. The initial wiring δ is again specified by the numbers in Figure 8. The wiring for c_0 is chosen in accordance with pin preassignments and the given wiring of the power supply nets. The number of vias induced by δ is 11.

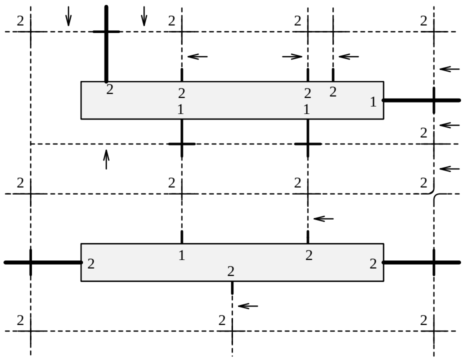

Figure 8: Circuit with power supply connections

The corresponding cluster graph is given in Figure 9. An optimum layer assignment δ' with 4 vias is obtained from δ by flipping the nodes of the maximum cut $X = \{1, 2, 3, 4, 7\}$. Figure 10 shows the planar embedding of the cluster graph obtained by the proof of Theorem 2. The nodes are placed inside the areas occupied by the corresponding clusters (indicated by shaded regions).

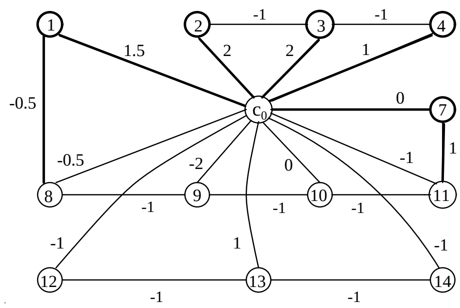

Figure 9: Cluster graph and maximum cut

5 Conclusion

In this paper the 2-layer *constrained via minimization problem with pin preassignments* (CVMPP) has been considered, which arises in the context of hierarchical wiring. Our results concerning CVMPP are twofold. On the one hand, they are destructive, since CVMPP has been proven to be NP-hard. It follows, that we can not expect to solve this optimization problem exactly in polynomial time, but have to restrict to approximation techniques [2].

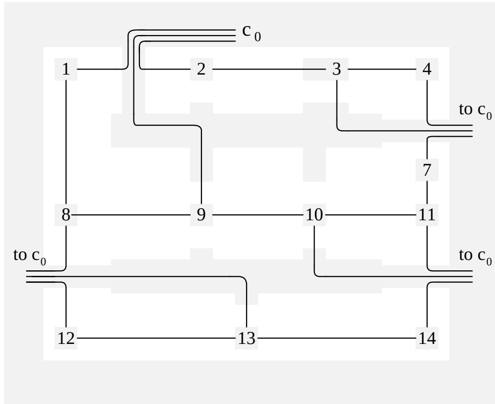

Figure 10: Planar embedding of cluster graph

On the other hand, we have seen that practical side constraints can drastically ease the problem. Thus, since vias on power supply connections are most expensive, the layer assignment for these connections is best fixed before 2-layer wiring of the signal nets is performed (in the case that both types of nets have to be embedded into the layers ALU1 and ALU2). It has been shown that under this constraint the CVMPP problem for the signal nets can be solved in time $O(n^{3/2} \log n)$, where n is the number of wire segments.

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